

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): NOGUCHI et al

Serial No.:

Filed: March 30, 2004

For: Semiconductor Integrated Circuit Device And
Fabrication Method For Semiconductor
Integrated Circuit Device

REAFFIRMATION OF CLAIM FOR PRIORITY

Mail Stop: Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

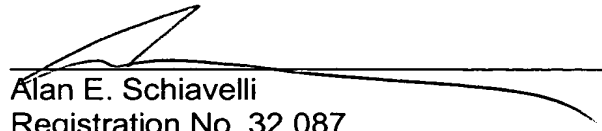
March 30, 2004

Sir:

Under the provisions of 35 USC §119 and 37 CFR §1.55, applicants hereby claim the right of priority based on Japanese Patent Application No. 2000-104015, filed in Japan on April 5, 2000.

The certified copy of the above-referred to Japanese Patent Application was filed on May 30, 2001 in prior application Serial No. 09/825,946, filed April 5, 2001.

Respectfully submitted,


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FORM PTO-1449 U.S. Department of Commerce
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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ATTY. DOCKET NO.

501.39932CX1

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GROUP

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	6 5 9 3 2 3 9	7/03	Kaufman			
	6 3 5 5 5 7 1	3/02	Huang			
	6 0 4 8 7 8 9	4/2000	Vines			
	6 3 4 8 4 0 2	2/02	Kawanoue			
	6 5 2 1 5 3 2	2/03	Cunningham			
	6 1 3 6 6 8 0	10/2000	Lai			
	6 2 4 2 3 4 9	6/01	Nogami			
	6 1 7 1 9 5 7	1/01	Maekawa			
	6 1 8 1 0 1 2	1/01	Edelstein			
	6 3 4 8 4 1 0	2/02	Ngo			
	6 1 5 9 8 5 7	12/2000	Liu			

FOREIGN PATENT DOCUMENTS

DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
					YES NO
10 1 5 4 7 0 9	1998	Japan			
11 0 8 7 3 4 9	1999	Japan			
11 0 8 7 5 0 9	1999	Japan			
11 2 2 0 0 2 3	1999	Japan			
11 0 1 6 9 1 2	1999	Japan			
10 2 6 1 7 1 5	9/98	Japan			

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

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	6 1 5 3 5 2 3	11/00	Van Ngo			
	6 1 9 1 0 0 7	2/01	Matsui			

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DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
					YES NO
6 2 2 4 1 9 4	8/94	Japan			
6 0 3 7 0 3 8	2/94	Japan			
9 0 8 2 7 9 8	3/97	Japan			

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